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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,521	03/23/2004	Won-Jin Kim	5649-1226	2748

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Laura M. Kelley
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428
Raleigh, NC 27627

EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,521	KIM ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-10 and 15* is/are rejected.

7)☒ Claim(s) *2-6,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed 7/01/2005.

Currently, claims 1-12 and 15 are pending.

Election/Restrictions

1. Applicant's election without traverse of claims 1-12 and 15 in the reply filed on 7/01/2005 is acknowledged.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

3. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

4. Claim 10 objected to under 37 CFR 1.75 as being a substantial duplicate of claim 9. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after

allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 7-10 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Sandhu et al. (U.S. Patent No. 6,090,708 dated 7/18/2000).

Sandhu shows the method as claimed in Figs. 1-11 and corresponding text as: forming at least one layer on a first (16) and a second side (14) of a semiconductor substrate (12); removing portions of the least one layer on the first side (25) (Fig. 11) of the semiconductor substrate to form a pattern of the least one layer on the first side of the substrate while maintaining the at least one layer on the second side of the substrate (col. 6, line 64- col. 7, line 19); forming a capping layer (20) on the pattern of the at least one layer on the first side of the substrate and on the at least one layer on the second side of the semiconductor substrate (col. 6, line 64- col. 7, line 19); removing the capping layer on the second side of the semiconductor substrate thereby exposing the at least one layer on the second side of the substrate while maintaining the capping layer on the first side of the substrate (col. 7, lines 20-28); removing the at least one layer on the second side of the semiconductor substrate, while maintaining the capping

layer and the pattern of the at least one layer on the first side of the semiconductor substrate (col. 7, lines 20-28); and removing a portion of the capping layer on the first side of the semiconductor substrate (col. 7, lines 29-40) (claim 1). Sandhu teaches that the capping layer is etched to form a contact pad (col. 6, line 64-col. 7, line 19) (claim 7). Sandhu teaches selectively etching a portion of the at least one layer to form a semiconductor structure on the first side of the semiconductor substrate (col. 7, lines 29-40) (claim 8). Sandhu teaches removing the capping layer on substantially the entire second side of the semiconductor substrate (col. 7, lines 20-28) (claims 9 and 10).

Sandhu shows the method as claimed in Figs. 1-11 and corresponding text as: forming a gate insulating layer on a first side (16) and a second side (14) of a semiconductor substrate (12) (col. 6, line 64-col. 7, line 19); forming a gate electrode layer (25 and 18) on the gate insulating layer on the first and the second sides of the semiconductor substrate (col. 6, line 64- col. 7, line 19); forming a masking layer on the gate electrode layer on the first and the second sides of the semiconductor substrate (col. 6, line 64-col. 7, line 19); patterning the gate insulating layer, the gate electrode layer and the masking layer on the first side of the semiconductor substrate to form a gate pattern on the first side of the semiconductor substrate while maintaining the gate insulating layer, the gate electrode layer, and the masking layer on the second side of the semiconductor substrate (col. 6, line 64-col. 7, line 19); forming a conductive layer (20) on the gate pattern and on the first side of the substrate and on the masking layer on the second side of the semiconductor substrate (col. 6, line 64-col. 7, line 19); removing the conductive layer on the second side of the semiconductor substrate

thereby exposing the masking layer (col. 7, lines 20-28); removing the masking layer, the gate electrode layer and the gate insulating layer on the second side of the semiconductor substrate while maintaining the conductive layer and the gate pattern on the first side of the semiconductor substrate (col. 7, lines 20-28); and removing a portion of the conductive layer on the first side of the semiconductor substrate to form contact pads between portions of the gate pattern (col. 7, lines 29-40) (claim 15).

Allowable Subject Matter

7. Claims 2-6 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein removing the capping layer on the second side of the semiconductor substrate further comprises applying an etching solution to the second side of the semiconductor substrate while applying a protective material to the first side of the semiconductor substrate to protect the first side from the etching solution, as required by claim 2; and

...wherein removing the at least one layer on the second side of the semiconductor substrate precedes removing a portion of the capping layer on the first side of the semiconductor substrate, as required by claim 11.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
September 15, 2005